Processing Wiegand Format Card Data

Reference Document

PXL-250

The PXL-250 Tiger Controller is capable of accepting Wiegand data from any Wiegand output device that meets the Security Industry Association's Wiegand Reader Interface Standard (SIA document number AC-01D-96). Keri Systems, Inc. cannot guarantee the performance and reliability of Wiegand devices that do not meet these guidelines. Use Table 1 for definitions of the abbreviations used throughout this document.

Abbreviation	Definition
D	data bit
E	data bit used for even parity comparison
FC	facility code bit
LSB	least significant bit – used for odd parity comparison
MSB	most significant bit – used for even parity comparison
O	data bit used for odd parity comparison
SIA	Security Industry Association
Tpi	pulse interval time
Tpw	pulse width time
Voh	voltage level for a high signal
Vol	voltage level for a low signal

Table 1 – Definition of Bit Abbreviations Used in this Document

The PXL-250 expects to receive 26 bits of Wiegand data in the order listed in Table 2.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
MSB	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	LSB

Table 2 – Expected Order for Receiving Wiegand Data

Of the 26 bits received, the most significant bit (MSB) and the least significant bit (LSB) are stripped off and used for parity checking of the remaining 24 bits (see Table 3). The MSB parity bit is checked for even parity with the upper 12 data bits. The LSB parity bit is checked for odd parity with the lower 12 data bits.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
MSB	E	E	E	E	E	E	E	E	E	E	E	E	O	O	O	O	O	O	O	O	O	O	O	O	LSB

Table 3 – Parity Processing Format

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If either even or odd parity checks fail, the data is ignored. If both even and odd parity checks pass, the remaining 24 data bits are separated into two groups: the facility code and the card identification code. Table 4 shows the breakdown of data bits.

2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
FC	FC	FC	FC	FC	FC	FC	FC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Table 4 – Separating Data into Facility Code and Identification Code

The first eight data bits (bits 2 through 9) are processed as the Facility Code and the last sixteen bits (bits 10 through 25) are processed as the card's identification code value. The current PXL-250 controller firmware combines the facility code value with the card identification code value to generate the card identification number used by the *Doors*™ access control program.

Figure 1 displays the timing pattern that is expected for data bits being received by the controller from the Wiegand device. The Data One and Data Zero signals should be held at a high voltage level (above the Voh level) until data is ready to be sent. Data is sent as low-going pulses (identified by the "saw-teeth" in Figure 1) on the Data One or Data Zero lines. Table 5 provides the minimum and maximum allowable pulse width times (the duration of the saw-tooth) and pulse interval times (the time between saw-teeth).

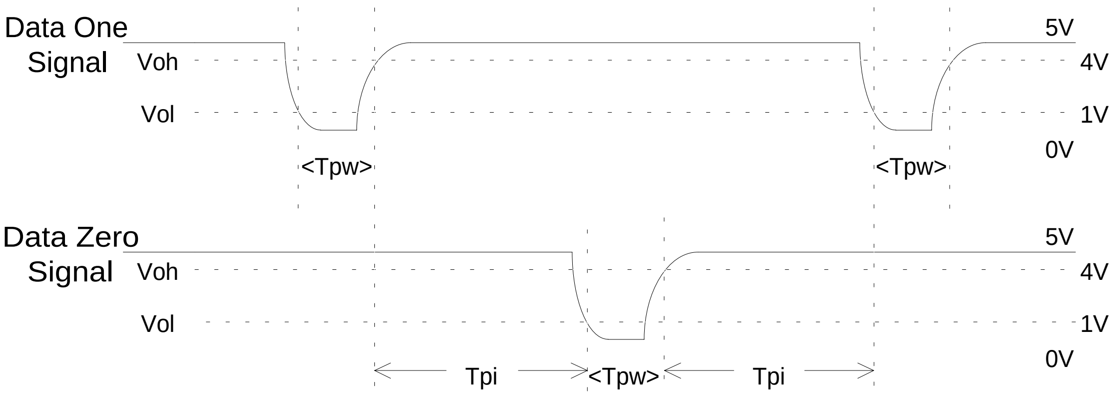

Figure 1 – Data Bit Timing Pattern

Symbol	Description	Minimum Time	Maximum Time
Tpw	Pulse Width Time	20 uS	100 uS
Tpi	Pulse Interval Time	200 uS	20 mS

Table 5 – Pulse Times